Irvine Sensors
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The company originally developed their stacking technology to support their sensor systems. The original DRAM stack is still available and is accompanied by SRAM and Flash. They are also producing a ceramic package based stack, a polyimide chip-on-board type stack and stacked TSOPs. These latter three technologies have not been evaluated by this program.

The **Stacked Memory Die** technology uses thin film technology to bring the contact from the surface of the die to the edge. The dice are stacked with adhesive and metallization is deposited on the outer surfaces to connect the dice. Several standard devices exist for DRAM, SRAM and Flash memory. The board interface is through wire bonding or by flip chip. They have also been offered in the past inside of an MCM package with a PGA interface.

NASA has used this stack in the Hubble Space Telescope Solid State Recorder. The SSR was successfully integrated into HST during the re-servicing mission in 1999. An investigation was done regarding the ability of the wire bonds to withstand the vibration environment. See
http://misspiggy.gsfc.nasa.gov/tva/Pkggen/wire/bondvibe.htm

The **TSOP Stack** is marketed for any TSOP device. The stack height is a maximum of 0.250". This is marketed for low cost and fast turn-around. Standard TSOP Stack products include:

1 Gbit Flash	Die is Samsung 16M X 8	0.824" x 0.532" x 0.460"
½ Gbit Flash	Same as 1Gbit above except 4 devices high instead of eight high	
¼ Gbit Flash	Same as 1Gbit above except 2 devices high instead of eight high	

The **Stacked Polyimide BGA** and **Stacked Ceramic BGA** have been discontinued but may be licensed for production in the future.

The **Neo-Stack™** is a stacked system which contains 11 different chips including the Intel StrongARM™ processor, IEEE 1394 interface chips, DRAM and Flash memory. It is bonded into a ceramic package whose board interface is tailorable. This product is marketed to the military and aerospace industries.